REMARKS

Claims 32, 40, 50, 51, 61 and 63 have been amended. Claims 32, 36, 38-40, 42, 44-48, 50-51, 60-61, and 63 remain pending. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the above-referenced application in light of the amendments and following remarks.

Applicants acknowledge with appreciation that claim 60 is in condition for allowance. Applicants also respectfully submit that claims 32, 36-40, 42, 44-48, 50-51, 59, 61, and 63 should also now be allowable in light of the amendments. In particular, as is explained below, independent claims 32, 40, 50, 51, 60, and 62 now recite "a metal layer formed over" a dielectric, insulating, or anti-reflective coating layer. At best, the primary reference Blatchford discloses a *photoresist* layer 16 is formed on the anti-reflective coating layer or dielectric layers.

Claims 36 and 63 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The rejection is respectfully traversed.

The Office Action asserts that there is no disclosure, in the original specification, of an integrated circuit comprising an additional (third) anti-reflective layer formed between the second anti-reflective layer and the dielectric layer, as recited in claim 36 (Office Action, p. 2). Applicants respectfully disagree.

In FIG. 3, three separate layers of anti-reflective coating material, *i.e.*, layers 12, 14, and 16, are formed between reflective layer 10 and photoresist layer 20, *i.e.*, a dielectric layer. Applicants also direct the Examiner's attention to Applicants' specification, p. 19, ll. 10-19, describing the three layers 12, 14, and 16. Consequently,

Applicants respectfully submit that claim 36 *is* supported by Applicants' specification and FIG. 3, and the § 112, first paragraph, rejection should be withdrawn.

Claim 63 has been amended to obviate the Examiner's concerns. Specifically, claim 63 now recites an integrated circuit comprising, "a reflective layer; a dielectric layer formed over the reflective layer; a first anti-reflective coating layer formed over the dielectric layer; at least a second anti-reflective coating layer formed on the first anti-reflective coating layer; and a metal layer formed over the at least second anti-reflective coating layer." Support is found in Applicants' specification, p. 21, ll. 2-12 and FIG. 8. Specifically, Applicants' specification provides that "it is possible to place *both* DARC layers 150, 152 *above* ILD layer 154." (p. 21, ll. 5-6) (emphasis added). Therefore, the rejection should be withdrawn.

Claim 63 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,713,234 ("Sandhu"). The rejection is respectfully traversed.

As indicated above, claim 63 has been amended to recite an integrated circuit comprising, "a reflective layer; a dielectric layer formed over the reflective layer; a first anti-reflective coating layer formed over the dielectric layer; at least a second anti-reflective coating layer *formed on* the first anti-reflective coating layer; and *a metal layer* formed over the at least second anti-reflective coating layer." (emphasis added).

As the Office Action acknowledges, Sandhu merely discloses that a silicon oxide film 58 is formed on the surface of interconnection layer 50, a first ARC 60 is formed on oxide film 58, a second dielectric layer 62 is formed on first ARC 60, and a second ARC 64 is formed on second dielectric layer 62. Sandhu does *not* disclose a second anti-reflective coating layer formed *on* the first anti-reflective coating layer,

much less *a metal layer* formed over an anti-reflective coating layer. Accordingly, the rejection should be withdrawn.

Claims 32, 36 and 38-39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No.: 6,200,734 ("Blatchford") in view of U.S. Patent No. 5,733,712 ("Tanaka"). The rejection is respectfully traversed.

At the outset, Applicants respectfully submit that claims 32 and 36-39 relate to an *integrated circuit* and *not* "a method for fabricating semiconductor devices in integrated circuits using photolithography" as the Office Action asserts (p. 4). Further, claim 32 recites an integrated circuit comprising, *inter alia*, "a dielectric layer formed on [the] second anti-reflective coating layer; and a *metal layer* formed over said dielectric layer." (emphasis added). Blatchford does not teach or suggest at least these features.

Blatchford discloses a structure with a metal layer 18, an anti-reflective coating structure 17 consisting of three separate layers 13-15, an optional oxynitride layer 19 formed on anti-reflective coating structure 17, and *a photoresist layer* 16 formed on oxynitride layer 19. Blatchford does not teach or suggest "a *metal layer* formed over said dielectric layer," as recited in claim 32. Blatchford's *photoresist layer* 16 is formed over the anti-reflective coating layers 13-15 and the optional oxynitride layer 19.

Tanaka is relied upon for disclosing known antireflection methods which utilize light interference to prevent reflection and that the reflectivity of interfaces be equal and of opposite phase in order to cancel the reflected light from those interfaces. Tanaka, however, does not add anything to rectify the deficiencies associated with Blatchford. Namely, both Blatchford do and Tanaka fail to disclose or suggest "a *metal layer* formed over said dielectric layer," as recited in claim 32.

As such, the cited references do not disclose or suggest an integrated circuit comprising, *inter alia*, "a reflective layer . . . a first anti-reflective coating layer formed over the reflective layer . . . a second anti-reflective coating layer formed over said first anti-reflective coating layer . . . a dielectric layer formed on said second anti-reflective coating layer; and a *metal layer* formed over said dielectric layer," as recited in claim 32 (emphasis added).

Claims 36 and 38-39 depend from claim 32 and should be allowable with claim 32 for at least the reasons provided above, and on their own merits. Specifically, the cited references do not teach or suggest "at least one additional anti-reflective coating layer formed *between* the second anti-reflective coating layer and the dielectric layer," as recited in claim 36 (emphasis added). The rejection should be withdrawn and the claims allowed.

Claims 40, 42, 44, 45, and 47-48 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blatchford in view of U.S. Patent No. 6,255,151 ("Fukuda"). The rejection is respectfully traversed.

For similar reasons provided above, Blatchford does not teach or suggest a memory cell comprising, *inter alia*, "an insulating layer formed on the second anti-reflective coating layer; and a *metal layer* formed over said insulating layer," as recited in claim 40 (emphasis added). Blatchford's *photoresist layer* 16 is formed over the anti-reflective coating layers 13-15 and the optional oxynitride layer 19.

Fukuda is relied upon for disclosing memory cells of a DRAM with an active region, gate oxide, gate electrode, word line, source/drain pair, capacitors, and a bit line. Fukuda, however, does not add anything to rectify the deficiencies associated

with Blatchford. Namely, the cited combination fails to disclose or suggest "a *metal layer* formed over said insulating layer," as recited in claim 40.

Moreover, Applicants respectfully submit that there is no motivation to combine Blatchford and Fukuda to arrive at the claimed invention. To establish a *prima facie* case of obviousness, a determination of obviousness "must involve more than indiscriminately combining prior art; a motivation or suggestion to combine must exist." *Pro-Mold & Tool Co.*, 75 F.3d at 1573.

In this case, there is no teaching, suggestion, or motivation to combine the cited references. For example, Blatchford is directed to the formation of an anti-reflective coating between a *non-planar substrate* and *a photoresist layer* "to alleviate the problems caused by non-uniform reflection at the substrate surface during exposure of the photoresist layer." (Abstract) (emphasis added). Fukuda, in contrast, relates to the creation of an offset between a cell array and a peripheral circuit region of a memory cell (Col. 1, l. 66 through Col. 2, l. 2). The only element in which Blatchford and Fukuda share is the semiconductor substrate on which their respective structures are formed. A person of ordinary skill in the art would not have been motivated to combine the cited references since the references are directed to solving entirely different problems.

"A statement that modifications of the prior art to meet the claimed invention would have been 'well within the ordinary skill of the art' at the time the claimed invention was made because the references relied upon teach that all aspects of the claimed invention were individually known in the art is *not sufficient* to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references." M.P.E.P. § 2143.02 (emphasis added). In this case, there is no objective reasoning to combine the cited references. It is impermissible hindsight reconstruction to combine the references.

Moreover, even if the references are properly combinable, which they are not, they still would not disclose or suggest a memory cell comprising, *inter alia,* "a structure on a substrate . . . [with] at least two active areas . . . a gate stack . . . a capacitor . . . a first anti-reflective coating layer . . . a second anti-reflective coating layer formed on at least a portion of the first anti-reflective coating layer . . . an insulating layer formed on the second anti-reflective coating layer; and *a metal layer* formed over said insulating layer," as recited in claim 40 (emphasis added).

Claims 42, 44-45, and 47-48 depend from claim 40 and should be allowable along with claim 40 for at least the reasons provided above, and on their own merits. Accordingly, the rejection should be withdrawn and the claims allowed.

Claim 46 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Blatchford and Fukuda, and further in view of U.S. Patent No. 6,140,179 ("Chen"). The rejection is respectfully traversed.

Claim 46 depends from claim 40 and should be similarly allowable along with claim 40 for at least the reasons provided above, and on its own merits. Specifically, Blatchford and Fukuda do *not* disclose or suggest a memory cell comprising, *inter alia,* "an insulating layer formed on [a] second anti-reflective coating layer; and *a metal layer* formed over said insulating layer," as recited in claim 40 (emphasis added). Blatchford's *photoresist layer* 16 is formed over the anti-reflective coating layers 13-15 and the optional oxynitride layer 19. Chen is relied upon for disclosing container capacitors and adds nothing to rectify the structural deficiencies of Blatchford and Fukuda.

Claim 50 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Blatchford in view of U.S. Patent No. 6,287,959 ("Lyons") and Fukuda. The rejection is respectfully traversed.

For similar reasons provided above, Blatchford and Fukuda do not teach or suggest the subject matter recited in claim 50. Specifically, Blatchford and Fukuda do not disclose or suggest an integrated circuit comprising, *inter alia,* "an insulating layer formed on the etch stop layer; and *a metal layer* formed over said insulating layer," as recited in claim 50.

Blatchford's *photoresist layer* 16 is formed over the anti-reflective coating layers 13-15 and the optional oxynitride layer 19. There is also no motivation to combine Blatchford and Fukuda since the references are directed to solving entirely different problems. Lyons is relied upon for disclosing that silicon oxynitride can be used as a successful etch stop, and adds nothing to rectify the structural deficiencies of Blatchford and Fukuda.

Moreover, even if the references are properly combinable, which they are not, they still fail to disclose or suggest a memory cell comprising, *inter alia,* "an etch stop layer comprising: a first anti-reflective coating layer formed over [a] structure; a second anti-reflective layer formed over at least a portion of the first anti-reflective coating layer; an insulating layer formed on the etch stop layer; and *a metal layer* formed over said insulating layer," as recited in claim 50. Accordingly, the rejection should be withdrawn and the claims allowed.

Claim 51 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Blatchford in view of Fukuda and U.S. Patent No. 5,724,299 ("Podlesny"). The rejection is respectfully traversed.

For similar reasons provided above, Blatchford and Fukuda do not teach or suggest the subject matter recited in claim 51. Specifically, Blatchford and Fukuda do not disclose or suggest a computer system comprising, *inter alia*, "a first anti-reflective coating layer formed over [a] first dielectric layer . . . a second anti-reflective coating layer formed over the first anti-reflective coating layer . . . a second dielectric layer formed over said second anti-reflective coating layer; and *a metal layer* formed over said second dielectric layer," as recited in claim 51.

Blatchford's *photoresist layer* 16 is formed over the anti-reflective coating layers 13-15 and the optional oxynitride layer 19. There is also no motivation to combine Blatchford and Fukuda since the references are directed to solving entirely different problems. Podlesny is relied upon for disclosing a memory cell array typically used as memory for a computer system, and adds nothing to rectify the structural deficiencies associated with Blatchford and Fukuda.

Moreover, even if the references are properly combinable, which they are not, they still fail to disclose or suggest a computer system comprising, *inter alia*, "a processor; and a memory, the memory comprising at least one memory cell, the memory cell comprising: a structure . . . at least two active areas . . . a gate stack . . . a capacitor . . . a first dielectric layer . . . a first anti-reflective coating layer formed over the dielectric layer . . . a second anti-reflective coating layer formed over the first anti-reflective coating layer . . . a second dielectric layer formed over said second anti-reflective coating layer; and *a metal layer* formed over said second dielectric layer," as recited in claim 51.

Applicants also respectfully submit that one of ordinary skill in the art would not have been motivated to combine the cited references with Podlesny to arrive at the subject matter of claim 51. For example, Blatchford addresses "problems caused by non-uniform reflection at the substrate surface during exposure of the photoresist layer" (abstract); whereas, Fukuda addresses the creation of an offset between the cell array and the peripheral circuit region of a memory cell; and, Podlesny addresses the formation of a cross-coupled sense amplifier as a storage element. The only element which all the references have in common is the substrate on which their respective structures are formed. Accordingly, the rejection should be withdrawn and the claims allowed.

Claim 61 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Blatchford in view of Lyons. The rejection is respectfully traversed.

As indicated above, Blatchford and Lyons do not teach or suggest an integrated circuit comprising, *inter alia*, "a dielectric layer formed over said reflective layer; and an etch-stop layer formed on the dielectric layer comprising: a first anti-reflective coating layer; a second anti-reflective coating layer formed over the first anti-reflective coating layer; and *a metal layer* formed over said second anti-reflective coating layer," as recited in claim 61 (emphasis added). Blatchford's *photoresist layer* 16 is formed over the anti-reflective coating layers 13-15 and the optional oxynitride layer 19. As discussed above, Lyons does not add anything to rectify the deficiencies associated with Blatchford. Accordingly, the rejection should be withdrawn and the claims allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to review and pass this application to issue.

Dated: September 12, 2005

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicants